REMARKS

Claims 39, 48, and 74 have been amended. Marked-up versions of amended claims 39, 48, and 74 are attached hereto. Claims 39, 41-48, 50-56 and 74-83 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 39 and 41-47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Laibowitz et al., U.S. Patent No. 6,088,216 (hereinafter "Laibowitz"), in view of Azuma et al., U.S. Patent No. 5,516,363 (hereinafter "Azuma"). The rejection is respectfully traversed.

Claim 39 has been amended to clarify that a capacitor with two sidewall regions having a thin film material with uniform stoichiometry is being claimed. Claim 39, as amended, recites a capacitor having two sidewall regions and "a post deposition doped BST high dielectric constant thin film material formed on at least both sidewall regions." According to the claim, the stoichiometry of said BST high dielectric thin film material is "substantially uniform at least at both sidewall regions." Applicant respectfully submits that Laibowitz and Azuma do not teach or suggest the claimed invention.

Laibowitz discloses a DRAM capacitor comprising a substrate 12, whereupon a mesa 51 and high dielectric film 56 are formed (Figure 7). However, Laibowitz fails to teach or suggest a capacitor in which the stoichiometry of the sidewalls is substantially uniform. Additionally, Laibowitz fails to disclose the importance of maintaining a uniform stoichiometry in the layer of thin film dielectric material on a sidewall. It should be noted that Laibowitz discloses a thin film material deposition technique and resulting structure upon which the claimed invention improves.

Although Azuma discloses a DRAM circuit that uses a "spin-on" technique to achieve a dielectric thin film 15 with uniform stoichiometry (Col. 18, lines 8-11), the Azuma reference fails to teach or suggest applying this method to a three-dimensional (3D) structure. The Azuma method requires that the substrate be spun "at about 1500 RPM

(the preferred range is about 1500-2000 RPM) for about 30 seconds" after the depositing step (Col. 18, lines 5-8). Indeed, the method taught by Azuma could not be applied to a 3D structure resulting in a capacitor with two sidewall regions having a high dielectric "thin film material formed at least on both sidewall regions" because it involves a "spin-on" step.

The combination of Laibowitz and Azuma structure would result in a structure depicted in attached Figs. A and B. Referring to Fig. A, the "spin-on" method disclosed by Azuma would result in an accumulation of the pre-doped precursor solution on a near raised sidewall, while not covering at all the far raised sidewall. In the case of a deep trench (Fig. B), the pre-doped precursor solution would accumulate at the far lowered sidewall, while failing to cover the near lowered sidewall. Therefore, it is not proper to combine Azuma and Laibowitz.

Since the "spin-on" method would not result in a "high dielectric constant thin film material formed at least on both sidewall regions," wherein the stoichiometry of the thin film material is substantially uniform, the combination of Azuma and Laibowitz fails to teach or suggest every limitation of claim 39. For at least this reason, Applicant respectfully submits that claim 39 is allowable.

Claims 41-47 depend from claim 39. Claims 41-47 contain every limitation of claim 39, and are allowable along with claim 39. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 48 and 50-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Laibowitz, in view of Azuma, and further in view of Leung et al., U.S. Patent No. 5,563,762 (hereinafter "Leung"). The rejection is respectfully traversed.

Claim 48, as amended, recites a capacitor with two sidewalls and "a post deposition doped BST high dielectric constant thin film material formed at least on both sidewall regions; wherein the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at both sidewall regions." A capping layer is also provided over at least a portion of said BST thin film material.

As noted above with respect to claim 39, Laibowitz and Azuma fail to teach or suggest a capacitor with two sidewalls and a "high dielectric constant thin film material formed at least on both sidewall regions," wherein the stoichiometry of the thin film material is substantially uniform at least at both sidewall regions. Leung discloses preparation of a capacitor whereby "a capping layer is deposited overall to encapsulate the capacitor structure" (Col. 2, line 46-49). Leung does not, however, disclose a capacitor with uniform stoichiometry of the BST high dielectric constant thin film material on the capacitor sidewalls. Accordingly, the combination of Laibowitz, Azuma and Leung fails to teach or suggest the subject matter defined in claim 48. For at least the foregoing reasons, claim 48 is allowable over the combination of Laibowitz, Azuma, and Leung.

Claims 50-56 depend from claim 48. Claim 50-56 contain every limitation of claim 48, and are allowable along with claim 48. Accordingly the rejection should be withdrawn and the claims allowed.

Claims 74-83 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hosotani et al., U.S. Patent No. 6,051,859 (hereinafter "Hosotani") in view of Azuma. The rejection is respectfully traversed.

Claim 74, as amended, recites a capacitor with two sidewalls and a "high dielectric constant thin film material formed at least on both sidewall regions," wherein the stoichiometry of the thin film material is substantially uniform at least at both sidewall regions. A second electrode is provided on the BST high dielectric thin film material.

As noted above with respect to claims 39 and 48, Azuma fails to teach or suggest a capacitor with two sidewalls and "high dielectric constant thin film material formed at least on both sidewall regions," wherein the stoichiometry of the thin film material is substantially uniform at least both sidewall regions. Although Hosotani teaches a capacitor comprising a substrate, first electrode, dielectric film, and second electrode, it does not teach or suggest a post deposition doped BST thin film material formed on at least both sidewall regions. Accordingly the combination of Azuma and Hosotani fails to teach or

suggest the subject matter defined in claim 74.For at least the foregoing reasons, claim 74 is allowable over the combination of Azuma and Hosotani.

Claims 75-83 depend from claim 74. Claims 75-83 contain every limitation of claim 74, and are allowable along with claim 74. Accordingly the rejection should be withdrawn and the claims allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Gianni Minutoli
Registration No.: 41,198
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700

Attorneys for Applicant

Version With Markings to Show Changes Made

In the Claims:

39. (Fourth Amended) A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by [a] at least two sidewall regions between said first and second levels; and

a post deposition doped BST high dielectric constant thin film material formed at least on [said] both sidewall regions;

wherein the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at [said] both sidewall regions.

48. (Fourth Amended) A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by [a] at least two sidewall regions between said first and second levels; and

a post deposition doped BST high dielectric constant thin film material formed at least on [said] both sidewall regions;

wherein the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at [said] both sidewall regions; and

a capping layer provided over at least a portion of said BST thin film material.

74. (Fourth Amended) An integrated circuit capacitor device comprising:

a material layer having a first level and a second level, said first and second levels being connected by [a] at least two sidewall regions between said first and second levels; and

a post deposition doped BST high dielectric constant thin film material formed at least on [said] both sidewall regions;

wherein the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at [said] both sidewall regions; and

a second electrode provided on said BST high dielectric thin film layer.